REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

As an initial matter, since the Examiner did not set a shortened statutory period for reply in the official action, no extension of time fee is due. The Examiner is requested to ensure that such an extension of time fee is not inadvertently charged by the USPTO for this response.

The Examiner's attention is also directed to a continuation-in-part application that claims priority from the instant application and a Serial Application No. 10/118,427 which is currently being examined by Examiner Luu in Group Art Unit 2128. A copy of the references recently cited by the Examiner in that application are submitted in an Information Disclosure Statement.

Claims 1-30 stand rejected under 35 U.S.C. §101 as allegedly being directed to non-statutory subject matter. This rejection is respectfully traversed.

With respect to claim 21, Applicant has amended that claim in accordance with the Examiner's suggestions. Accordingly, the rejection of claim 21 should now be moot.

Applicant respectfully traverses the rejection of claims 1 and 11 which are clearly statutory under the standard articulated by the Federal Circuit *in State Street Bank.* They are also statutory in view of the recently-issued decision *Ex parte Lundgren* in which the Board of Patent Appeals and Interferences issued a precedential opinion eliminating the Patent Office policy of rejecting patent applications under 35 U.S.C. §101 as being outside of the "technological arts." A brief review of claims 1 and 11 of the instant application indicates that they are directed to statutorily-recognized subject matter classes with claim 1 being directed to an apparatus and claim 11 being directed to a method. Both claims recite entities, which can be implemented using hardware or software, to provide a new, useful, concrete, and tangible result.

Claims 1 and 11 are directed to simulating data processing operation systems as part of verifying or testing the design of those data processing systems. Indeed, system-on-chip (SoC) designs which integrate a large number of functional elements on a single integrated circuit require significant amounts of validation and testing before the designs can be reliably released for manufacture. This validation and testing requirement is a bottleneck in getting new systems into the market place. The apparatus and method recited in claims 1 and 11, respectively, improve the efficiency and effectiveness of such validation and testing designs--a highly useful, concrete, and tangible result. Applicant notes that the Examiner quotes the language "any useful, concrete or tangible **product**." The *State Street Bank* test articulated by the Federal Circuit specifies a useful, concrete, and tangible *result*--and not a product. *State St. Bank & Trust Co. v. Signature Fin. Group, Inc.*, 149 F.3d 1368 (Fed. Cir. 1998). Here, claims 1 and 11 clearly produce such a useful, concrete, and tangible result--improved validation and testing of IC designs. Whether implemented by hardware or by software running on hardware is irrelevant to the fact that the elements in claims 1 and 11 produce a useful, concrete, and tangible result. *AT&T v. Excel Communications, Inc.*, 172 F.3d 1352 (Fed. Cir. 1999). Withdrawal of the rejections under 35 U.S.C. §101 is respectfully requested.

All claims 1-30 stand rejected under 35 U.S.C. §102 as being anticipated by U.S. Patent 6,678,645 to Rajsuman et al. This rejection is respectfully traversed.

The Examiner will note that the subject matter of claim 2 has been incorporated into claim 1, the subject matter of claim 13 into claim 11, and the subject matter of claim 23 into claim 21. With respect to rejecting the subject matter of claim 3, the Examiner refers to column 12, lines 29-33 of Rajsuman.

In Rajsuman, a software application is broken up into multiple sub-tasks scheduled and assigned to different verification units, which the Examiner contends are counterparts of the claimed signal interface controllers. The cited passage in Rajsuman discloses that a control central processing unit (CPU), an arbitration unit, and a synchronization clock unit allow data transfer from a main system CPU 62 to the control the CPUs of the individual verification units. See Figure 9. But this passage neither discloses nor suggests:

> said tests scenario manager includes a shared data memory into which a signal interface controller may store data using a test scenario controlling message sent from said signal interface controller to said test scenario manager, said data being readable from said shared data memory by at least one of: (i) another signal interface controller; (ii) said test scenario manager.

The main system CPU 62, which the Examiner contends is the counterpart of the claimed test scenario manager, does not store data on behalf of one of the verification units (interface controllers) in response to a message sent by that verification unit to the main system CPU 62. Nor does Rajsuman disclose that data is stored in a shared memory by one of the verification units. Rajsuman further lacks a shared memory that is readable by at least one of (i) another one of the verification units, and (ii) the main system CPU 62. Because multiple claim features are absent from Rajsuman, the anticipation rejection should be withdrawn.

These distinguishing features are significant. A signal interface controller may store data in the shared memory using the test scenario controlling message sent from the signal interface controller to the test scenario manager. The data stored in this shared memory is readable by at least one of a different one of the plurality of signal interface controllers and the test scenario manager. The shared data memory approach allows a signal interface controller to provide feedback, such as trace results, including error messages and observed responses, and also allows

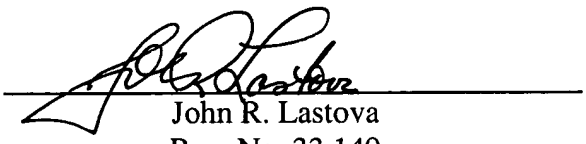
further signal interface controllers to read data by another signal interface controller and then respond to that data. This is a valuable and powerful technique suitable for point-to-point validation testing operations.

In contrast to this use of a shared memory, Rajsuman emphasizes that there is a one-to-one relationship between the verification units and the silicon ICs, which the Examiner equates with the hardware simulator. See column 8, lines 40 to 41. This one-to-one mapping between verification units and silicon ICs *teaches away* from using a shared data memory.

The application is in condition for allowance. An early notice to that effect is requested.

Respectfully submitted,

NIXON & VANDERHYE P.C.

By: 
John R. Lastova
Reg. No. 33,149

JRL:sd
901 North Glebe Road, 11th Floor
Arlington, VA 22203-1808
Telephone: (703) 816-4000
Facsimile: (703) 816-4100